The Extensible Translating Instruction Set Simulator (ETISS)
HWFault Tolerance Analysis

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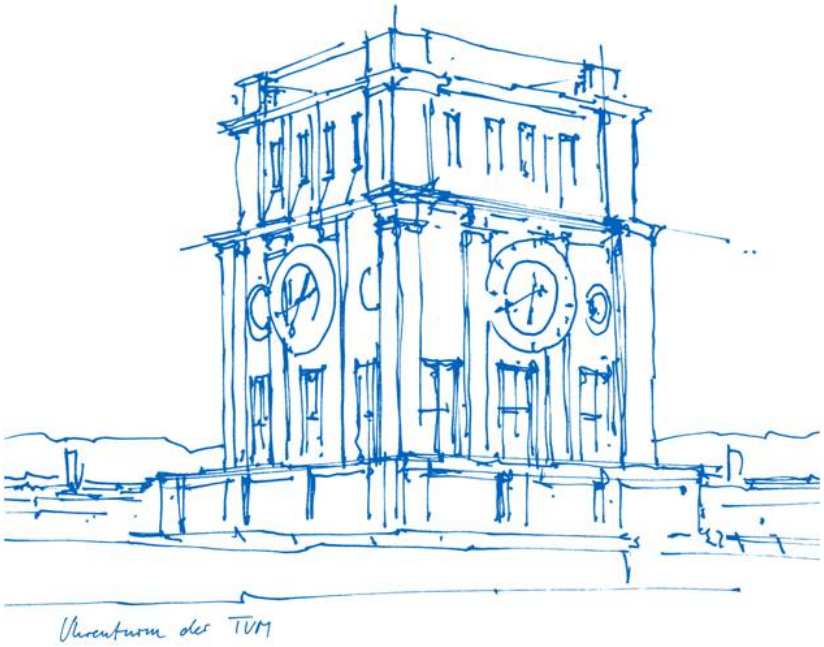
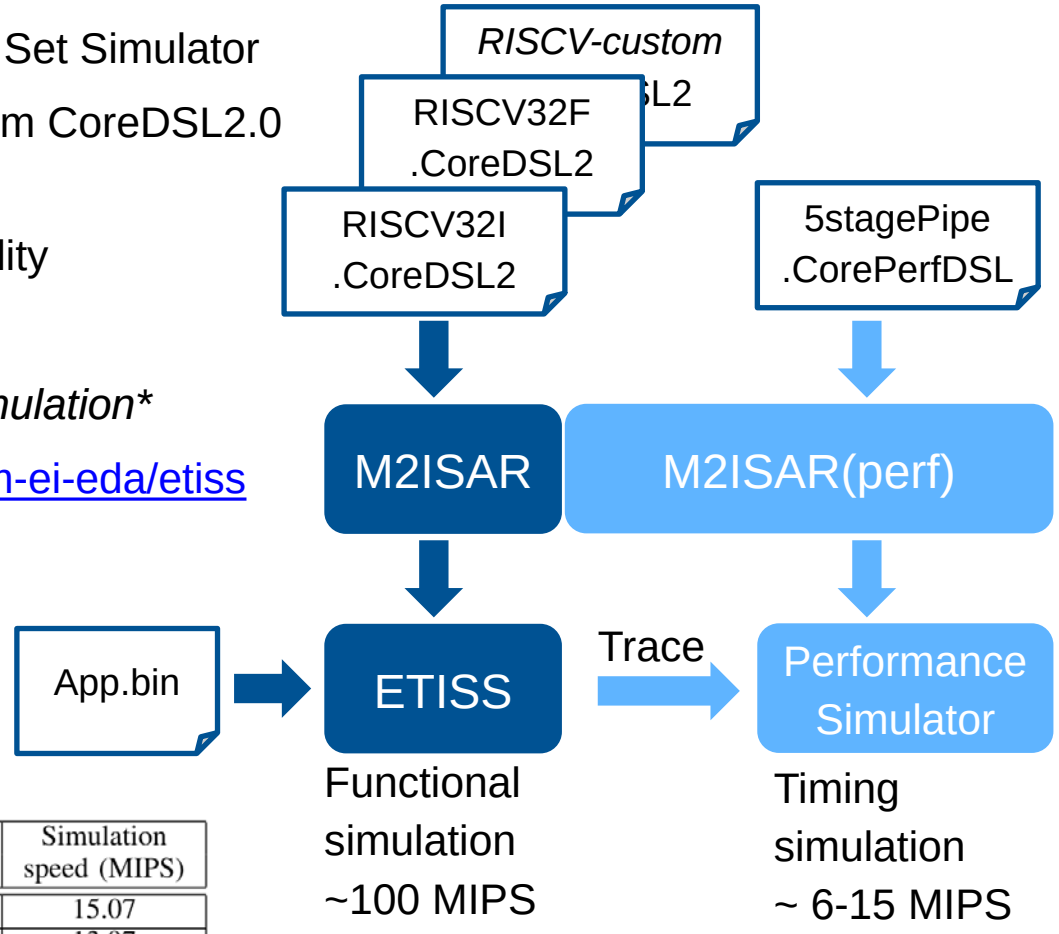


2022 DAC Open Source BoF Meeting

ETISS Simulator

- ETISS: ISA-independent Instruction Set Simulator
- M2ISAR: Generates Architecture from CoreDSL2.0 files (ISA description language)
- Plug-in Mechanism to add functionality
- RISC-V support
- *Ongoing work: Add performance simulation**
- Open Source: https://github.com/tum-ei-eda/etiss



Dhyrstone Benchmark
5-stage Pipeline

Architecture	Forwarding	Branch prediction	Est. target perf. (CPI)	Simulation speed (MIPS)
Harvard	No	No	1.59	15.07
		Static	1.52	13.97
		Dynamic	1.48	12.27
	Yes	No	1.23	15.09
		Static	1.15	13.92
		Dynamic	1.11	12.72

**To appear in FDL23*

Recent ETISS Uses in Research

- Profiling Post-Quatum Crypto Algorithms [2]
- Fault Injection – Evaluation of Software-Implemented HW Fault Tolerance Methods [3]
- Profiling and tuning ML kernels for RISC-V [1]

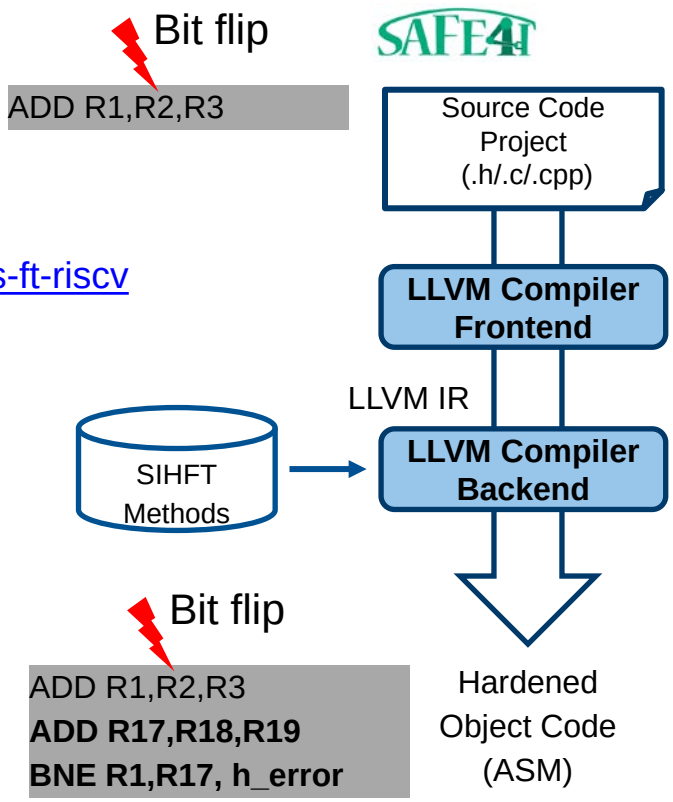
[1] Bringing TinyML to RISC-V With Specialized Kernels and a Static Code Generator Approach
Rafael Stahl
Embedded World Conference 22
[2] Exploring the risc-v vector extension for the classic McEliece post-quantum cryptosystem
S Pircher, J Geier, A Zeh, D Mueller-Gritschneder
ISQED21
[3] REPAIR: Control Flow Protection based on Register Pairing Updates for SW-Implemented HW Fault Tolerance
U Sharif, D Mueller-Gritschneder, U Schlichtmann
TECS20

Software-Implemented HW Fault Tolerance (SIHFT)

COMPAS Compiler
- Builds redundancy into the generated code for soft error resilience
- based on LLVM Infrastructure
- Open Source: https://github.com/tum-ei-eda/compas-ft-riscv

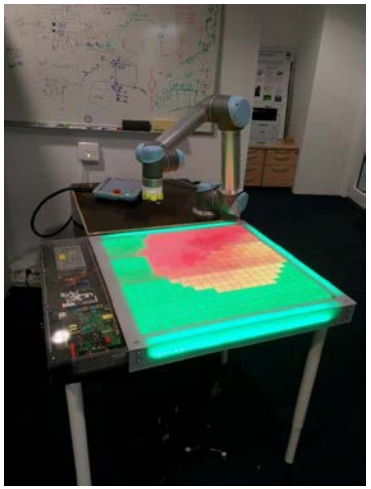
Ported well known SIHFT methods to RISC-V
- **CFCSS**, **RASM** for control-flow hardening
- **EDDI**, **SWIFT**, **NZDC** for data-flow hardening

Novel **REPAIR** transformation
- Adapt data-flow hardening to also cover control-flow errors

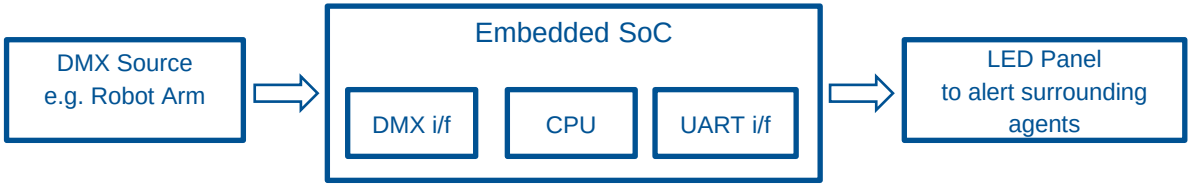


U Sharif, D Mueller-Gritschneder, U Schlichtmann
COMPAS: Compiler-assisted Software-implemented Hardware Fault Tolerance for RISC-V
11th Mediterranean Conference on Embedded Computing (MECO), 2022
.

Case Study with Embedded DMX Decoder



- Embedded System setup to decode the DMX packet stream to control LED panel (SystemC Virtual Prototyping)



REPAIR Performance Evaluation

	unprotected	nzdc_fgs	nzdc_cgs	nzdc_cgs + CFCSS	nzdc_cgs + RASM	nzdc_cgs + **REPAIR**
SDC-rate	1.778%	0.196%	0.186%	0.078%	**0.064%**	**0.067%**
overheads	1x	2.46x	2.46x	3.21x	**3.15x**	**2.66x**

U Sharif, D Mueller-Gritschneder, U Schlichtmann
REPAIR: Control Flow Protection based on Register Pairing Updates for SW-Implemented HW Fault Tolerance
ACM Transactions on Embedded Computing Systems (TECS), 2021
.

Further Open Source Projects

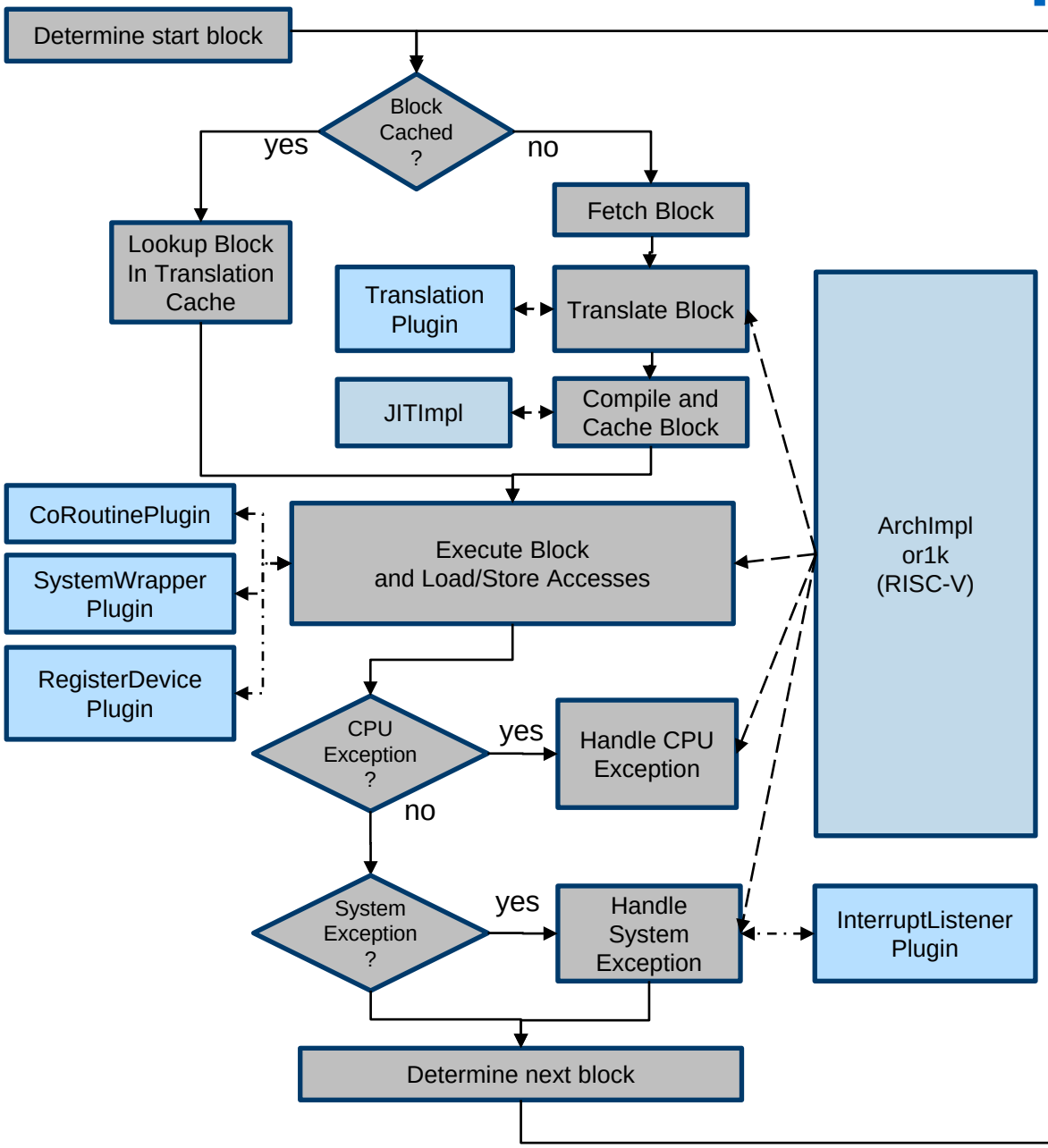
- ML Kernels for RISC-V Micro-Controllers: https://github.com/tum-ei-eda/muriscv-nn
- TinyML Deployment with TVM: https://github.com/tum-ei-eda/mlonmcu

TUM. Technische Universität München

Extendable Translating Instruction Set Simulator (ETISS)

- **So why another ISS?**
  1. Copyleft licenses (GPL) for open-source approaches such as Qemu
     - ➢ Problem for integration in industrial VPs
  2. Commercial approaches such as ARM fast models are closed-source.
     - ➢ Hard to integrate custom functionality or share
- **ETISS‘s key features:**
  - ISA-independent Instruction Set Simulator (ISS)
  - Fast Dynamic Binary Translation (DBT) based on C as intermediate format
  - Easy integration in SystemC/TLM VPs
  - Open License Model (TBD: Under consideration is Apache License)
  - Advanced plugin-mechanism:
    - ➢ Easy to integrate new functionality such as tracing/debugging/timing models without „hacking“ the simulation loop

ETISS Simulation Loop



Plugin Types

- **TranslationPlugin**:
  - Called when new block is translated.
  - Can add more translation code, e.g. instruction counter, tracing, timing models
- **CoRoutinePlugin**:
  - Called before new block is executed.
  - Can react on external events e.g., interrupts, user input , faulit injection trigger, etc.
- **SystemWrapperPlugin**:
  - Called before accesses memory.
  - Can be used to model memory-mapped devices
- **InterruptListenerPlugin**:
  - Called when interrupt is received.
- **RegisterListenerPlugin**:
  - Notification when CPU registers are updated.
  - Can be used to model devices that are controlled by special-purpose registers of the processor.
- **ISA Plugin ArchImpl**:
  - Used to model processor ISA and architecture.
  - Atm support for or1k, RISC-V, ARM M0
- **JIT Plugin**:
  - Compiler plugin to translate C to host machine.
  - Atm support for LLVM, gcc, and tcc (Tested on Ubuntu 14 and Ubuntu16)